admits that Yamamoto fails to teach "cooling the wafer and a heat treatment of a batch furnace."

Thus, Yamamoto, as described in the Abstract and on page 5, lines 8-18, of the present specification, only discloses a method wherein a wafer is subjected to a single heat treatment in an atmosphere containing hydrogen using either a batch processing type furnace (see Yamamoto, Fig. 2) or a rapid thermal annealing (RTA) treatment (see Fig. 4) after the delaminating step to planarize its delaminated surface.

To cure the deficiency in the teaching of Yamamoto, the Office Action cites Takada. Takada teaches forming an insulating layer; implanting hydrogen ions into the semiconductor surface; joining the semiconductor substrate to a support substrate; delaminating the resulting structure through heat treatment; and subjecting the delaminated structure to an additional heat treatment. Furthermore, Takada teaches that the laminate is subjected to a thermal treatment under a pressure of 1×10^{-6} to 1×10^{-11} Torr at a temperature of 900 to 1200 °C to planarize the surface of the SOI layer. The Office Action asserts that the combination of Takada and Yamamoto teaches annealing by using either a batch furnace or by rapid thermal annealing (RTA). Thus, the Office Action concludes that it would have been obvious to one of ordinary skill in the art to use either type of heat treatment for the first part of a heating step and the other for the rest of the heating step. Applicants disagree.

Applicants respectfully submit that the claimed invention would not have been obvious over the cited references. A feature of the claimed method for producing an SOI wafer according to claim 1 is that "after a delamination step, a wafer having an SOI layer is subjected to a two-stage heat treatment in an atmosphere containing hydrogen or argon utilizing a rapid heating/rapid cooling apparatus and a batch processing type furnace" (emphasis added). Such a method would not have been obvious over a combination of the cited references.

As described on page 8, lines 1-11 of the present specification, "if a wafer having an SOI layer is subjected to a heat treatment consisting of two stages utilizing separately a rapid heating/rapid cooling apparatus and a batch processing type furnace after the delamination as described above, surface crystallinity is restored and the surface roughness of short periods is improved in the heat treatment by the rapid heating/rapid cooling apparatus, and the surface roughness of long periods can be improved by the heat treatment utilizing the batch processing type furnace." In addition, at page 6, lines 1-17, the present specification clearly indicates that "when the inventors of the present invention precisely investigated the improvement of the surface roughness of an SOI wafer by RTA, it was found that only short period components of surface roughness were improved to a level comparable to that of mirror-polished wafers... and long period components were still extremely inferior to those of the mirror polished wafers." Neither reference, alone or in combination, teaches or suggests any such benefits being provided by a two-step heating process, as claimed.

According to the claimed invention, the wafer is subjected to a two-stage heat treatment in an atmosphere containing hydrogen or argon utilizing a rapid heating/rapid cooling apparatus and a batch processing type furnace. This process provides significant and unexpected results not taught or suggested by the references. The improved surface roughness properties are apparent in Table 1 and Table 2 of the present specification. As described in Examples 1 and 2, each wafer was subjected to a two-stage heat treatment including heat treatment by an RTA apparatus and heat treatment by a batch processing type furnace (see Table 1). As a result, the surface roughness for both of 1 μm square (short periods) and 10 μm square (long periods) was significantly improved after the heat treatment (see Table 2).

In contrast, the wafer of Comparative Example 1, which was only subjected to the heat treatment by the RTA apparatus, shows improvement only in the RMS value for 1 μm

square, but still possessed an RMS value for 10 μm square that was significantly larger than those of the wafers in Examples 1 and 2. Thus, it can be seen that the long period components of surface roughness were not improved sufficiently. (See Table 2).

In both Yamamoto and Takada et al., the wafer is only subjected to a single heat treatment either by RTA or in a batch processing type furnace. In contrast, the claimed invention requires a two-stage heat treatment utilizing both a rapid heating/rapid cooling apparatus and a batch processing type furnace. In addition, neither Yamamoto nor Takada teaches or suggests that the surface roughness of short periods can be improved by heat treatment in a rapid heating/rapid cooling apparatus and that the surface roughness of long periods can be improved by heat treatment in a batch processing type furnace.

Furthermore, the thermal treatment step taught by Takada is performed under a pressure of 1×10^{-6} to 1×10^{-11} Torr, which is essentially a vacuum. Thus, the heat treatment taught by Takada does not occur in an atmosphere containing hydrogen or argon as in the claimed invention.

Thus, the combined teachings of Yamamoto and Takada neither teach nor suggest combining a heat treatment utilizing an RTA apparatus with an additional heat treatment utilizing a batch processing type furnace. The teachings of the combined references also fail to provide any motivation to one of ordinary skill in the art to utilize the two-step heat treatment as claimed, as neither reference suggests any advantages of such a treatment process. The asserted combination and modification by the Office Action could only be made in light of Applicants disclosure, which amounts to the use of impermissible hindsight on the part of the Patent Office.

Because the references neither teach nor suggest that the surface roughness of short periods can be improved by heat treatment utilizing an RTA treatment and the surface roughness of long periods can be improved by heat treatment utilizing a batch processing

type furnace, one of ordinary skill in the art would not have been able to conceive the claimed method. Thus, Yamamoto and Takada fail to provide any motivation to one to purposely subject a wafer to a two-stage heat treatment in an atmosphere containing hydrogen or argon utilizing RTA and a batch processing type furnace, as claimed.

Moreover, even if the teachings of these references are combined with each other, the invention of claim 1 of the present application cannot be derived therefrom. As discussed above, in both Yamamoto and Takada, a wafer having an SOI wafer is only subjected to a single heat treatment by either RTA or a batch processing type furnace. Thus one of ordinary skill in the art would not have been able to derive the claimed invention, where an SOI wafer is subjected to a two-stage heat treatment in an atmosphere containing hydrogen or argon by RTA and a batch processing type furnace based on the combined teachings of Yamamoto and Takada.

For at least these reasons, claims 1 and 2 would not have been obvious over the cited references. Reconsideration and withdrawal of this rejection are respectfully requested.

B. Yamamoto and Takada et al. further in view of admitted prior art and Wolf et al., Silicon Processing for the VLSI Era, Vol. 1, (1986) Lattice Press, pp. 23-25.

Claims 3-5 are rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Yamamoto and Takada, and further in view of the admitted prior art discussed in the specification and Wolf et al. Applicants respectfully traverse this rejection.

The Office Action cites and applies Yamamoto and Takada as described above. However, the Office Action admits that the combination of Yamamoto and Takada fails to teach that CZ wafer, in which crystal originated particles (COPs) at least on the surface are reduced, is used as the bond wafer and that the CZ wafer is produced from a single crystal ingot. The Office Action asserts that Wolf discloses that the CZ wafer can be produced form a single crystal ingot. The Office Action also asserts that the admitted prior art discloses a

CZ wafer of which the COPs at least on the surface are reduced is used as the bond wafer. Thus, the Office Action asserts it would have been obvious to one of ordinary skill in the art to employ the CZ wafer taught by Wolf and the admitted prior art.

Applicants respectfully submit that the claimed invention would not have been obvious over the cited references. A feature of the method for producing an SOI wafer according to claim 3 of the present application is that "an FZ wafer, an epitaxial wafer or a CZ wafer of which COPs at least on surface are reduced is used as the bond wafer, and the wafer having an SOI layer is subjected to a heat treatment under an atmosphere containing hydrogen or argon in a batch processing type furnace after the delamination step." In addition, claim 4 requires that "a CZ wafer produced from a single crystal ingot of which COPs are reduced for the whole crystal is used as the bond wafer." These features, in combination with the rest of the claim limitations, are not taught or suggested by the cited references.

The Office Action asserts that Wolf, at pages 23-25, teaches that the CZ wafer can be produced from a single crystal ingot and that on pages 4-5 of the present specification, the admitted prior art discloses the use of a CZ wafer in which COPs at least on surface are reduced as the bond wafer. Thus, the Office Action concludes that it would have been obvious to one of ordinary skill in the art to employ the CZ wafer of the admitted prior art and/or Wolf to provide the bond wafer of the combination. Applicants disagree.

Contrary to the assertions of the Office Action, the prior art described on pages 4-5 of the present specification does not disclose the use of a CZ wafer in which COPs at least on the surface are reduced as the bond wafer. In particular, from page 4, line 4, to page 5, line 7, of the instant specification, the method taught in Japanese Patent Laid-open (Kokai) Publication No. 10-275905 is described. The Japanese publication indicates that hydrogen annealing may be used to improve the surface roughness of a thin SOI layer. However, the

instant specification teaches that if the SOI layer (i.e., bond wafer) is formed from a CZ wafer and has a thickness of about 0.5um or less, the COPs that typically exist in a CZ wafer penetrate the SOI layer and form pinholes. Thus the buried oxide layer is etched during hydrogen annealing, which markedly degrades the electric characteristics of the wafer. Although the discussed art describes improving the surface roughness of an SOI layer, or the like, using a heat treatment, it does not teach or suggest the use of a bond wafer as in the claimed invention. Wolf only discloses a method of producing a silicon wafer from a single crystal ingot, and fails to teach or suggest the improvement in surface roughness of an SOI layer.

Therefore, although a typical dual CZ wafer may be used as a bond wafer and the surface roughness of an SOI layer, or the like, may be improved by heat treatment after delamination, one of ordinary skill in the art would not have been able to derive the claimed invention based on the teachings of Yamamoto and Takada taken in view of Wolf or the admitted prior art. In other words, a CZ wafer in which COPs at least on the surface are reduced or a Cz wafer obtained from a single crystal ingot in which COPs are reduced for the whole crystal has never been used as a bond wafer. Accordingly, claims 3 and 4, and Claim 5, which further limits claim 4, cannot have been derived from the cited references and the alleged Applicant's admitted prior art.

Thus, the citation of Wolf or the admitted prior art described in the specification by the Office Action fails to cure the deficiency in the teaching of Yamamoto and Takada, described in detail above.

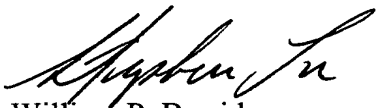
For at least these reasons, claims 3-5 would not have been obvious over the cited references. Reconsideration and withdrawal of this rejection are respectfully requested.

II. Conclusion

In view of the foregoing remarks, Applicants submit that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-5 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,



William P. Berridge
Registration No. 30,024

Stephen Tu
Registration No. P-52,304

WPB/SXT:amw

Date: June 14, 2002

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461